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<b>TRANSMITTAL FORM</b> <i>(to be used for all correspondence during pendency of filed application)</i>	Application Number	10/606,419	
	Filing Date	June 26, 2003	
	First Named Inventor	Vigyan Singhal	
	Group Art Unit Number	2825	
	Examiner Name	Tuyen P. To	
Total Number of Pages in This Submission	36	Attorney Docket Number	24006-08742

ENCLOSURES (check all that apply)	
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REMARKS:

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Signature:		
Attorney/Reg. No.:	John T. McNelis, Reg. No. 37,186	Dated: 6 Jan 2006

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PATENT

IN THE UNITED STATES  
PATENT AND TRADEMARK OFFICE

APPLICANT(S): Vigyan Singhal *et al.*  
APPLICATION NO.: 10/606,419  
FILING DATE: June 26, 2003  
TITLE: System and Method for Guiding and Optimizing Formal Verification  
for a Circuit Design  
EXAMINER: Tuyen P. To  
GROUP ART UNIT: 2825  
ATTY. DKT. NO.: 24006-08742

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LETTER TO THE CHIEF DRAFTSPERSON

SIR:

In response to the drawing informalities indicated on the Office Action Summay for the above-entitled patent application, please substitute the enclosed 11 sheet(s) of formal drawings containing Figures 6-16 for the 11 sheet(s) of drawings containing Figures 6-16 previously submitted.

Respectfully submitted,  
Vigyan Singhal *et al.*

Dated: 6 Jan 2006

By: [Signature]  
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